QN8066

Digital FM Transceiver for Portable Devices

General Description

The QN8066 is a high performance, low power, fully integrated single-chip stereo FM transceiver designed for PMP/PNDs, and portable radios, wireless microphone and other consumer electronics. It integrates both FM receiving and transmitting functions, auto-seek and clear channel scan, and antenna tuning to ease matching in real applications. Advanced digital architecture enables superior receiver sensitivity, crystal clear audio.

With its small footprint, minimal external component count and multiple clock frequency support, the QN8066 is easy to integrate into a variety of small form-factor low power portable applications. An integrated voltage regulator enables direct connection to a battery and provides high PSRR for superior noise suppression. A low-power Standby mode extends battery life. ESD protection is on all pins. The QN8066 is fabricated in highly reliable CMOS technology.

Key Features

- **Worldwide FM Band Receive and Transmit**
  - *60 MHz ~ 108 MHz full band tuning in 50/100/200 kHz step sizes*
  - *50/75μs pre-emphasis and de-emphasis*
- **High Performance FM Receiver (FMR)**
  - *Superior sensitivity: 1.2 μV_{EMF}*
  - *High SNR: 63dB Stereo*
  - *Ultra-low THD: 0.04%*
  - *High interference rejection*
  - *Integrated adaptive noise cancellation (SNC, HCC, SM)*
  - *Auto tuning support*
- **Stereo Earphone Driving with Line in feature**
  - *In Line-in mode, audio input feed into earphone driver directly, save external earphone driver*
- **1 kHz Tone Generator Inside**
- **High Performance FM Transmitter (FMT)**
  - *62dB Stereo SNR, 0.04% THD*
  - *Maximum 119 dBμV RF output level with 42dB adjustable range*
  - *Integrated Clear Channel Scan*
- **Automatic Input Audio Sensing**
  - *RF power automatically turned off if no input audio signal for 60s*
- **RDS/RBDS Transmit & Receive**
  - *Supports US and European data service, including TMC (Traffic Messaging Channel)*
  - *High speed RDS mode*
- **Very Low Power Consumption**
  - *9.2mA (Transmit Mode), 13.5mA (Receive Mode)*
  - *Power saving IDLE and STANDBY modes*
  - *Low shutdown leakage current*
- **Ease of Integration**
  - *Small footprint 4.9 × 6.0mm SSOP16*
  - *Low cellular and GPS band spurs*
  - *32.768 kHz and multiple MHz clocks input*
  - *I^2C control interfaces*
  - *VCC: 1.8~5.0V, integrated LDO, support battery direct connection. Accommodate 1.6~3.6V digital interface*
- **Robust Operation**
  - *-25^0C to $+85^0C$ operation*
  - *ESD protection on all input and output pads*

Typical Applications

- Portable Audio & Media Players
- Wireless microphone
- Netbooks
- Automotive Accessories

CONTENTS

REVISION HISTORY

REVISION	CHANGE DESCRIPTION	DATE
0.1	Draft	2013-8-10
0.2	Use new logo; Solder Reflow Profile: 1.6 mm<thickness<2.5 mm in Table 4-, Pb-Free Process - Classification Temperatures (Tc) of IPC/JEDEC J-STD-020D; Sensitivity note: . Lab test sensitivity ranged at -114.3~ -108dBm, but -101dBm at 85.5MHz.	2013-8-19

STATEMENT:

Users are responsible for compliance with local regulatory requirements for low power unlicensed FM broadcast operation. Quintic is not responsible for any violations resulting from user's intentional or unintentional breach of regulatory requirements in personal or commercial use.

1 FUNCTIONAL BLOCK DIAGRAM

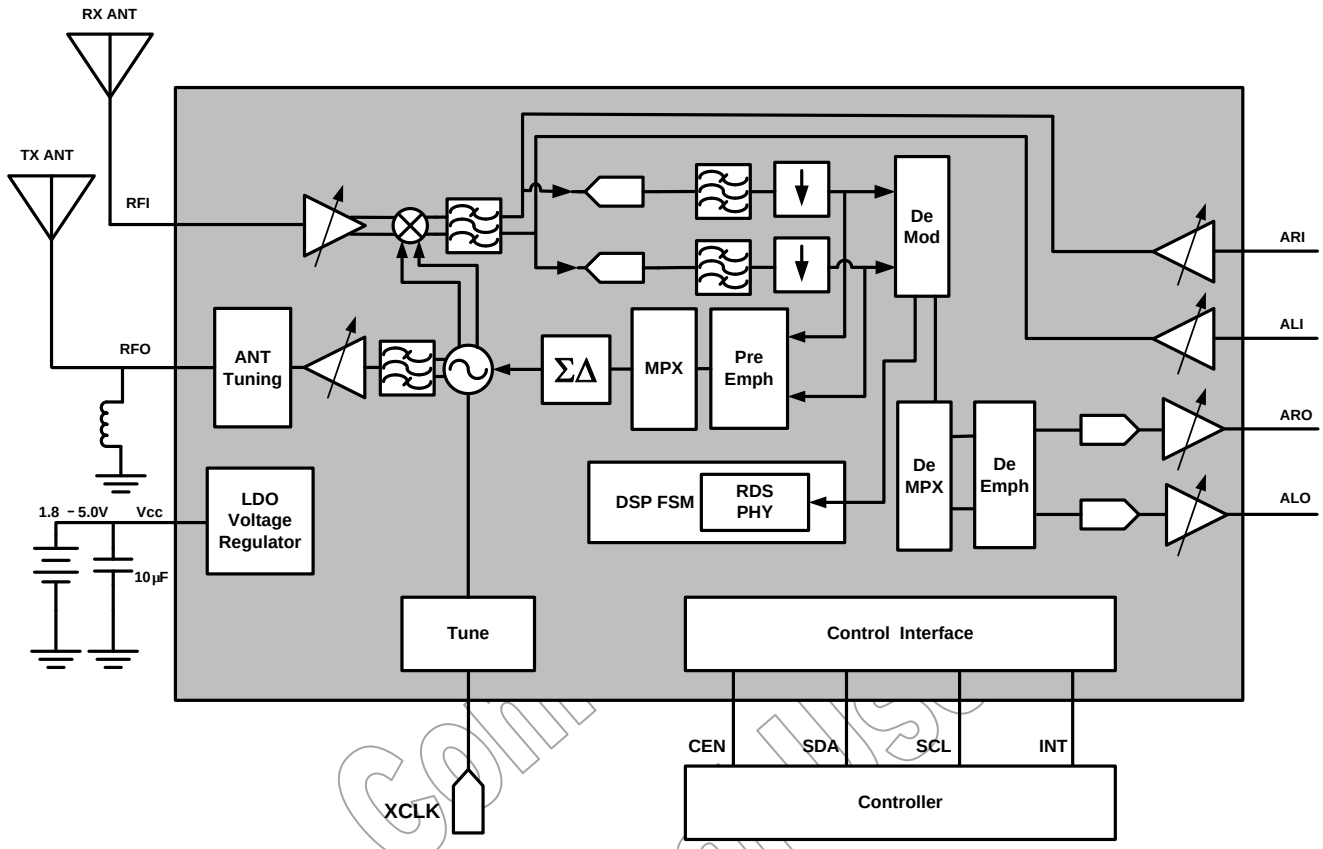


Figure 1 QN8066 Functional Blocks

2 PIN ASSIGNMENTS

(Top View)

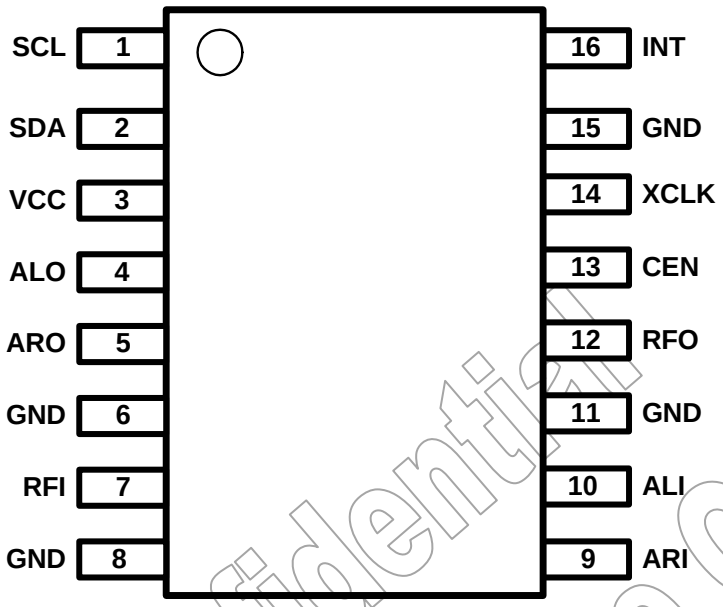


Figure 2 QN8066-UCNB Device Pin out

Table 1: Pin Descriptions

SSOP16	NAME	DESCRIPTION
3	VCC	Voltage supply.
4	ALO	Analog audio output – left channel.
5	ARO	Analog audio output – right channel.
6	GND	Ground.
7	RFI	FM Receiver RF input.
8	GND	Ground.
9	ARI	Right channel audio input.
10	ALI	Left channel audio input.
11	GND	Ground.
12	RFO	Transmitter RF output – connect to matched antenna.
13	CEN	Chip enable with internal pull up: Chip power down if less than 0.4V and VIO is powered; power up if higher voltage or left floated.
14	XCLK	External clock input.
15	GND	Ground.
16	INT	Interrupt output, active low, need pull-up externally.

1	SCL	Clock for I^2C serial bus.
2	SDA	Bi-directional data line for I^2C serial bus.

3 ELECTRICAL SPECIFICATIONS

Table 2: Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNIT
V_{bat}	Supply voltage	VCC to GND	-0.3	5	V
V_{IO}[1]	Logic signals level	CEN, SCL, SDA, to GND	-0.3	3.6	V
T_s	Storage temperature		-55	+150	^oC

Notes:
1. V_{IO} is pulled up externally via resisters

Table 3: Recommended Operating Conditions

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Vcc	Supply voltage	VCC to GND	1.8	3.3	5.0	V
T_A	Operating temperature		-25		+85	^oC
V_{ain}	L/R channel input signal level	Single ended peak to peak voltage		1000	2000	mV
RF_{in}	RF input level[1]	Peak input voltage			0.3	V
V_{IO}[2]	Digital I/O voltage		1.6		3.6	V

Notes:
1. At RF input pin, RFI;
2. V_{IO} is pulled up externally via resisters.

Table 4: DC Characteristics

(Vcc = 1.8 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V, f carrier=88 MHz and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
I_{RX}	Receive mode supply current	analog audio interface		13.5		mA
I_{TX}	Transmit mode supply current[1]	analog audio interface	9.2		15.5	mA
I_{IDLE}	Idle mode supply current	Idle mode		1		mA
I_{STBY}	Standby mode supply current	Standby mode		84		µA
I_{PDN}	Power down leakage current	power down		12		µA
Interface						
V_{OH}	High level output voltage		0.9*V_{IO}			V
V_{OL}	Low level output voltage				0.1*V_{IO}[2]	V
V_{IH}	High level input voltage		1.7 or 0.7*V_{IO}			V
V_{IL}	Low level input voltage				0.3	V

Notes:
1. Max: RFO output level is 119 dBµV, Min: RFO=82 dBµV;
2. V_{IO} is pulled up externally via resisters.

Table 5: AC Characteristics

(Vcc = 1.8 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.30V and T_A = 25°C).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
F_{xtal}	Clock frequency	Real-Time Clock	0.032768 -40[1]			MHz
F_{xtal_err}	Crystal frequency accuracy in RX mode	Over temperature, and aging	-20		20	ppm
	Crystal frequency accuracy in TX mode		-50		-50	

Notes:
1. See also XTAL_DIV0/ XTAL_DIV1/ XTAL_DIV2 (register 07h, 08h, 09h)
2. FCC requires ± 2 kHz worst case carrier offset, then the accuracy should be within ± 20 ppm.

Table 6: Transmitter Characteristics

(Vcc = 1.8 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V, f carrier=88 MHz and T_A = 25°C).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
R_{audio_in}	Audio input impedance	At pin ALI and ARI	10		80	kΩ
C_{audio_in}	Audio input capacitance[1]	At pin ALI and ARI		2	5	pF
G_{audio_In}	Audio input gain	RIN[1:0] = 10	-9		6	dB
ΔG_{audio_In}	Audio gain step	For any gain setting		1		dB
τ_{emph}	Pre-emphasis time constant[1]	PETC = 1	71.3	75	78.7	μs
		PETC = 0	47.5	50	52.5	
SNR_{audio_tx}	Tx audio SNR[3]	MONO, Δf = 22.5 kHz		53		dB
		STEREO, Δf = 68.25 kHz, Δf_{pilot} = 6.75 kHz		62		
THD_{audio_tx}	Tx audio THD[3]	STEREO, Δf = 68.25kHz, Δf_{pilot} = 6.75 kHz		0.04		%
α_{LR_tx}	L/R separation [2, 3]			43		dB
B_{LR_tx}	L/R channel imbalance [1, 2]	L and R channel gain imbalance at 1 kHz offset from DC			1	dB
M_{pilot}	19 kHz pilot modulation [2, 3, 6]	Relative to 75 kHz deviation	7	9.0	15	%
SUP_{sub}	38 kHz sub-carrier [2, 3] suppression		88			dB
C_{tune}	Output capacitance tuning range[1]		5		30	pF
P_{out}	RF output voltage swing[4]	RF Channel frequency = 88 MHz	88		119	dBμV
ΔG_{RF_Out}	Power gain step	Over process, temperature	0.7	1.5	2.5	dB
ΔP_{out}	Power gain flatness	Over 60 MHz ~ 108 MHz	-2		2	dB
P_{mask}	RF output spectrum mask[5]	120 kHz to 240 kHz offset		-43	-35	dBc
		240 kHz to 600 kHz offset		-50	-43	
		>600 kHz offset			-43	
F_{rf}	RF channel frequency		60		108	MHz
F_{ch}	Channel frequency step		50	100	200	kHz
F_{err}	Channel center frequency accuracy		-2		2	kHz
F_{perr}	Pilot Tone frequency accuracy[1]		-2		2	Hz
F_{pk}	Modulation peak frequency deviation			75		kHz
Notes:						

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT

1. Guaranteed by design;
2. Stereo (TX_MONO=0 Reg01h, bit 4);
3. 1000mVp-p, 1 kHz tone at ALI pin, no input signal at ARI pin;
4. Into matched antenna (see application note for details);
5. Within operating band 60 MHz to 108 MHz;
6. Value set with GAIN_TXPLT[3:0] (Reg 27h, bit[3:0]). The user must conform to local regulatory requirements for low-power unlicensed FM broadcast operation when setting this value.

Table 7: Receiver Characteristics

(Vcc = 1.8 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V, f carrier=88 MHz and T_A = 25°C).

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT
S_{RX}	FM sensitivity	(S+N)/N = 26dB		1.2[2]		μV_{EMF}
S_{RDS}	RDS sensitivity	BER≤5%, average over 2000 blocks		8.9		μV_{EMF}
IP3	Input referred IP3	At maximum gain		103		dBμV
Rej_{AM}	AM suppression			72		dB
R_{in}	RF input impedance	At pin RFI		5		kΩ
S_{RX_Adj}	Adjacent channel rejection	200 kHz offset		51		dB
S_{RX_Alt}	Alternate channel rejection	400 kHz offset		60		dB
SNR_{audio_in}	Audio SNR	MONO, Δf = 22.5 kHz[1]		58		dB
		STEREO, Δf = 68.25 kHz, Δf_{pilot} = 6.75 kHz		63		
THD_{audio_in}	Audio THD	MONO, Δf = 68.25 kHz		0.03		%
		STEREO, Δf =68.25 kHz, Δf_{pilot} = 6.75 kHz		0.04		%
α_{LR_in}	L/R separation			45		dB
Att_{Pilot}	Pilot rejection			66		dB
B_{LR}	L/R channel imbalance	L and R channel gain imbalance at 1 kHz offset from DC			1	dB
τ_{emph}	De-emphasis time constant[1]	PETC = 1	71.3	75	78.7	μs
		PETC = 0	47.5	50	52.5	μs
V_{audio_out}	Audio output voltage	Peak-Peak, single ended		0.8		V
R_{LOAD}	Audio output impedance		32			Ω
C_{audio_out}	Audio output capacitance				20	pF
$RSSI_{err}$	RSSI uncertainty		-3		3	dB
THD_{driver}	Audio THD after earphone driver	R_{LOAD}=32Ω, 1 V_{pp} output		0.15		%
		R_{LOAD}=1kΩ, 1 V_{pp} output		0.03		
Notes:						

SYMBOL	PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNIT

1. Guaranteed by design
2. Lab test sensitivity ranged at -114.3~ -108dBm, but -101dBm at 85.5MHz.

Table 8: Timing Characteristics

(Vcc = 1.8 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
τ_{pup}	Chip power-up time [1]	From rising edge of CEN to PLL settled and transmitter ready for transmission.			0.6	Sec
τ_{chsw}	Channel switching time[1]	From any channel to any channel.			0.1	Sec
Transmitter Timing						
τ_{wkup}	Wake-up time from standby to transmit			25	200	msec
τ_{CCS}	Clear channel scan time	Per channel.		50		msec
Receiver Timing						
τ_{wkup}	Wake-up time from standby to receive	Standby to RX mode.		200		msec
τ_{trx}	Mode switch time from receive to/from transmit	RX mode to TX mode.		500		µsec
		TX mode to RX mode.		100		msec
τ_{tune}	Tune time	Per channel, including Seek [1].		50		msec

Notes:
1. Guaranteed by design.
2. More time is required until audio is output.

Table 9: I²C Interface Timing Characteristics

(Vcc = 1.8 ~ 5.0 V, T_A = -25 ~ 85 °C, unless otherwise noticed. Typical values are at Vcc = 3.3V and T_A = 25°C).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	I²C clock frequency				400	kHz
t_{LOW}	Clock Low time		1.3			µs
t_{HI}	Clock High time		0.6			µs
t_{ST}	SCL input to SDA falling edge start [1,3]		0.8			µs
t_{STHD}	SDA falling edge to SCL falling edge start[3]		0.8			µs
t_{rc}	SCL rising edge[3]	Level from 30% to 70%			300	ns
t_{fc}	SCL falling edge[3]	Level from 70% to 30%			300	ns
t_{dtHD}	SCL falling edge to next SDA rising edge[3]		20			ns
t_{dtc}	SDA rising edge to next SCL rising edge[3]				900	ns
t_{stp}	SCL rising edge to SDA rising edge [2,3]		0.6			µs
t_w	Duration before restart[3]		1.3			µs
C_b	SCL, SDA capacitive loading[3]			10		pF

Notes:
1. Start signaling of I²C interface.
2. Stop signaling of I²C interface.
3. Guaranteed by design.

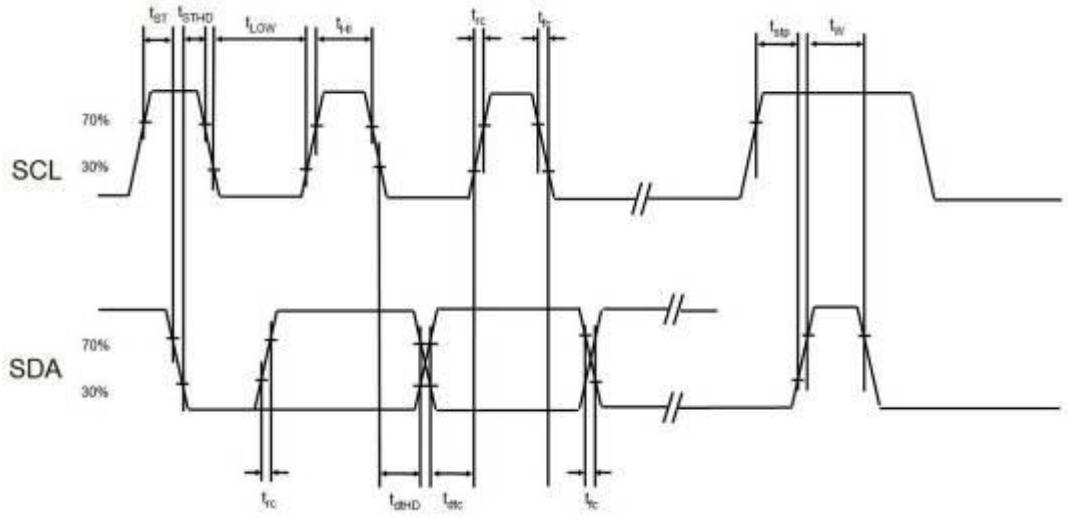


Figure 3 I²C Serial Control Interface Timing Diagram

4 FUNCTIONAL DESCRIPTION

The QN8066 is a high performance, low power, single chip FM transceiver IC that supports worldwide FM broadcast band operation. It has transmit/receive modes for normal broadcasting/tuning as well as IDLE and STANDBY modes for saving power. RDS/RBDS data service is also supported in both transmit and receive modes.

4.1 Transmit Mode

The QN8066 transmitter uses a highly digitized architecture. The input left and right analog audio signals are first adjusted by two automatic gain controlled (AGC) amplifiers, and then digitized by two high resolution ADCs into the digital domain. Pre-emphasis, soft clipping and MPX encoding are then performed. If RDS mode is enabled, the RDS signal will also be mixed with the MPX signal and the combined output will be fed into a high performance digital FM modulator which generates FM signal at RF carrier frequency. The FM signal is then filtered and amplified by the PA.

The QN8066 can deliver up to 119dBμV output signal to an external antenna and/or matching network. An RF VGA provides 42 dB of output power control range in 1.5dB steps and can be programmed through the serial control bus. Output power control and in-band power flatness can be easily achieved by a calibration circuit. This wide range of control allows for various antenna configurations such as loop, monopole, or meandering traces on PCB. An integrated RF bandpass filter ensures optimal output spectral purity.

4.2 Receive Mode

The QN8066 receiver also uses a highly digitized low-IF architecture, allowing for the elimination of external components and factory adjustments.

The received RF signal is first amplified by an integrated LNA and then quadrature down-converted to IF. An integrated IF channel filter then rejects out-of-channel interference signals. AGC is also performed simultaneously to optimize the signal to noise ratio as well as linearity and interference rejection. The filtered signal is digitized and further processed with a digital FM demodulator and MPX decoder. Audio processing is then performed based on received signal quality and channel condition. Two high-quality audio DACs are integrated on chip and will be used as an analog interface. The RDS signal will also be decoded if RDS reception is enabled.

4.3 Idle and Standby Mode

The QN8066 features low power IDLE and STANDBY modes for fast turn around and power saving. After power up, the QN8066 will enter STANDBY mode automatically.

4.4 Analog Audio Interface

The QN8066 has a highly flexible analog audio interface and integrates 32 ohm headphone audio driver. In transmit mode, for audio input, the signal is AC coupled with a 3dB corner frequency less than 50Hz. It has 4 different input impedances and 15 dB adjustable gain range (in 1 dB step) to optimize the SNR and linearity. The gain setting can be controlled automatically by integrated AGC or manually set through serial interface.

In receive mode, the single ended audio output level is 1V peak to peak and will be AC coupled to external audio driver.

4.5 Audio Processing

The QN8066 supports both transmit and receive mode audio processing.

In transmit mode, audio AGC, programmable pre-emphasis, and soft clipping are supported. The AGC state machine will detect the signal level and control the VGA gain to optimize both SNR and THD. A saturation indicator is also integrated which will be asserted when the input signal is out of the range of AGC. A soft clipping feature provides graceful performance degradation when the signal level is higher than a pre-determined level.

Stereo signal is generated by the MPX circuit. It combines the left and right channel signals in the following way:

$$m(t) = [L(t) + R(t)] + [L(t) - R(t)]\sin(4\pi ft + 2\theta_0) + \alpha\sin(2\pi ft + \theta_0) + d(t)\sin(6\pi ft + 3\theta_0)$$

Here, L(t) and R(t) correspond to the audio signals on left and right channels respectively, f = 19 kHz, θ is the initial phase of pilot tone and α is the magnitude of pilot tone, and d(t) is RDS signal. In mono mode, only the L+R portion of audio signal is transmitted. The 19 kHz pilot tone is generated by the MPX circuit which contributes 9% of peak modulation, and RDS signal will contribute 2.1% of peak modulation.

In receive mode, stereo noise cancellation (SNC), high cut control (HCC) and soft mute (SM) are supported. Stereo noise suppression is achieved by gradually combining the left and right signals to be a mono signal as the received signal quality degrades. SNC, HCC and SM are controlled by SNR and multipath channel estimation results.

Pre-emphasis and de-emphasis functions are also integrated with both 75μs and 50μs time constants. The time constant can be programmed through the serial control interface.

4.6 Channel Setting

The QN8066 supports both auto tuning/scan and manual channel settings.

Manual Channel Setting

By programming channel index RXCH[9:0] or TXCH[9:0], the RF channel can be set to any frequency between 60 MHz ~ 108 MHz in 50 kHz steps. The channel index and RF frequency have the following relationship:

F_{RF} = (60 + 0.05 x Channel Index), where F_{RF} is the RF frequency in MHz.

Clear Channel Scan

The QN8066 can automatically find the clearest channel and return the channel information for FM transmission. The start, stop and frequency step of searching, as well as upward or downward searching, can be programmed through the serial interface.

Auto Tuning

In receive mode, the QN8066 can automatically tune to stations having good signal quality. The start, stop and frequency step of tuning, as well as upward or downward tuning, can be programmed through the serial interface.

4.7 RDS/RBDS

The QN8066 supports RDS/RBDS data transmitting and receiving, including station ID, Meta data, TMC information, etc. The integrated RDS processor performs all symbol encoding/decoding, block synchronization, error detection and correction functions. RDS/RBDS data communicates with an external MCU through the serial control interface.

When the chip is used as an FM receiver, the internal RDS buffer (the entire RDS Group (8 bytes) is full, and an Interrupt signal is generated. The signal waveform is shown in Figure 4. The user can also check the RDS buffer space by reading the RDS_RXUPD bit in the STATUS2 register (reg. 17h [7]).

When the chip is used as an FM transmitter (RDS TX), ping-pong buffers are used so that the user can write into one buffer while the RDS data in the other buffer is being transmitted. When the internal RDS buffer (8 bytes) is full, an Interrupt signal is generated. The signal waveform is shown in Figure 4. The user should wait for the Interrupt signal (INT) before toggling the RDSRDY bit in the SYSTEM2 register (reg. 01h [1]). Alternatively, the user can also check the RDS buffer space by reading the RDS_TXUPD bit in the STATUS2 register (reg. 1Ah [2]).

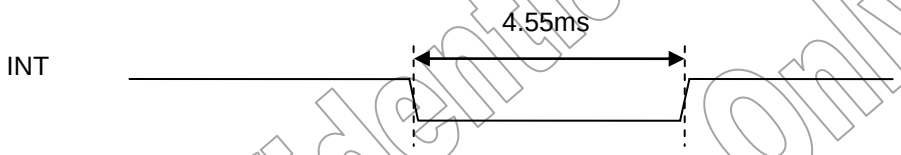


Figure 4 Interrupt Output

Notes:

1. INT should be pulled up externally.

5 CONTROL INTERFACE PROTOCOL

The QN8066 supports the standard I²C serial interfaces. At power-on, all register bits are set to default values.

I²C Serial Control Interface

QN8066 provides an I²C-compatible serial interface. It consists of two wires; serial bi-directional data line (SDA) and input clock line (SCL). It operates as a slave on the bus, and the slave address is 0100001. The data transfer rate on the bus is up to 400 Kbit/s.

SDA must be stable during the high period of SCL, except for start and stop conditions. SDA can only change with SCL being low. A high-to-low transition on SDA while SCL is high indicates a start condition. A low-to-high transition on SDA while SCL is high indicates a stop condition.

An I²C master initiates a data transfer by generating a start condition followed by the QN8066 slave address, MSB first, followed by a 0 to indicate a write cycle. After receiving an ACK from the QN8066 (by pulling SDA low), the master sends the sub-address of the register, or the first of a block of registers it wants to write, followed by one or more bytes of data, MSB first. The QN8066 acknowledges each byte after completion of each transfer. The I²C master terminates the write operation by generating a stop condition (P).

The read operation consists of two phases. The first phase is the address phase. In this phase, an I²C master initiates a write operation to the QN8066 by generating a start condition (S) followed by the QN8066 slave address, MSB first, followed by a 0 to indicate a write cycle. After receiving ACK from the QN8066, the master sends the sub-address of the register or the first of a block of registers it wants to read. After the cycle is acknowledged, the master terminates the cycle immediately by generating a stop condition (P).

The second phase is the data phase. In this phase, an I²C master initiates a read operation to the QN8066 by generating a start condition followed by the QN8066 slave address, MSB first, followed by a 1 to indicate a read cycle. After an acknowledge from the QN8066, the I²C master receives one or more bytes of data from the QN8066. The I²C master acknowledges the transfer at the end of each byte. After the last data byte to be sent has been transferred from the QN8066 to the master, the master generates a NACK followed by a stop.

The timing diagrams below illustrate both write and read operations.

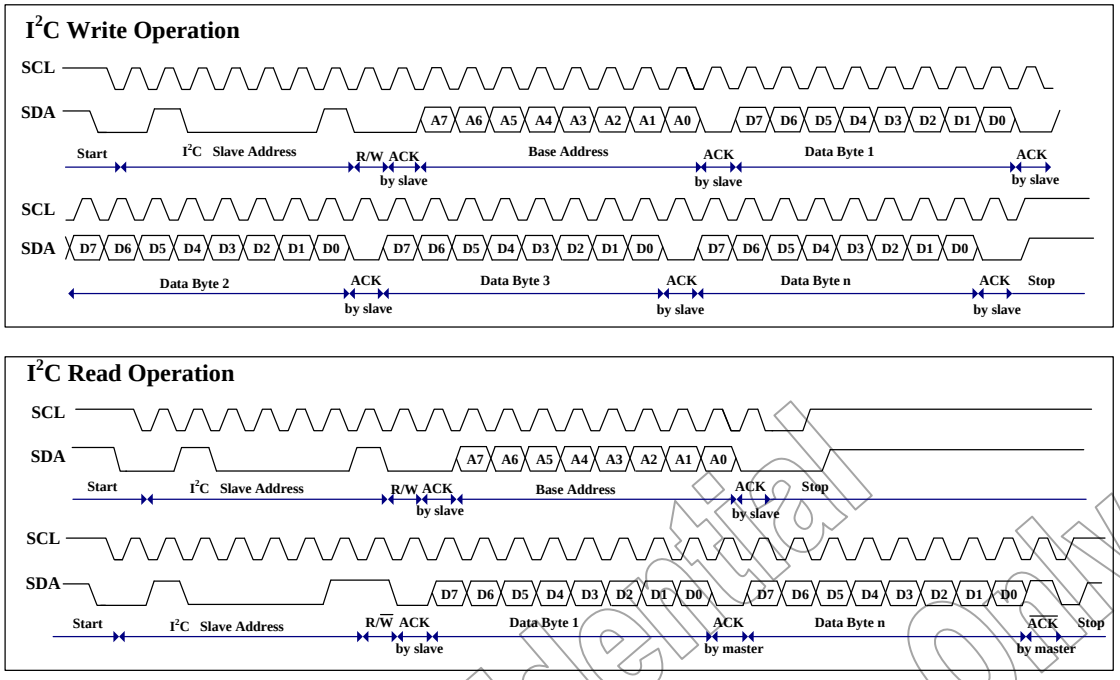


Figure 5 I²C Serial Control Interface Protocol

Notes:

1. The default IC address is 0100001.
2. "42" for a WRITE operation, "43" for a READ operation.

6 USER CONTROL REGISTERS

-------- THIS IS A PREVIEW LIST. Number and content of registers subject to change without notice --------

There are 41 user accessible control registers. All registers not listed below are for manufacturing use only.

Table 10: Summary of User Control Registers

REGISTER	NAME	USER CONTROL FUNCTIONS
00h	SYSTEM1	Sets device modes.
01h	SYSTEM2	Sets external clock type and CCA parameters.
02h	CCA	Sets CCA parameters.
03h	SNR	Estimate RF input CNR value
04h	RSSISIG	In-band signal RSSI dBμV value.
05h	CID1	Device ID numbers.
06h	CID2	Device ID numbers.
07h	XTAL_DIV0	Frequency select of reference clock source.
08h	XTAL_DIV1	Frequency select of reference clock source.
09h	XTAL_DIV2	Frequency select of reference clock source.
0Ah	STATUS1	System status.
0Bh	RX_CH	Lower 8 bit of 10-bit receiver channel index.
0Ch	CH_START	Lower 8 bits of 10-bit channel scan start channel index.
0Dh	CH_STOP	Lower 8 bits of 10-bit channel scan stop channel index.
0Eh	CH_STEP	Channel scan frequency step. Highest 2 bits of receiver channel indexes.
0Fh	RX_RDSD0	RDS data byte 0.
10h	RX_RDSD1	RDS data byte 1.
11h	RX_RDSD2	RDS data byte 2.
12h	RX_RDSD3	RDS data byte 3.
13h	RX_RDSD4	RDS data byte 4.
14h	RX_RDSD5	RDS data byte 5.
15h	RX_RDSD6	RDS data byte 6.
16h	RX_RDSD7	RDS data byte 7.
17h	STATUS2	Receiver RDS status indicators.
18h	VOL_CTL	Audio volume control.
19h	INT_CTRL	Receiver RDS control
1Ah	STATUS3	Receiver audio peak level and AGC status.
1Bh	TXCH	Lower 8 bit of 10-bit transmitter channel index.
1Ch	TX_RDSD0	Transmit RDS data byte0.
1Dh	TX_RDSD1	Transmit RDS data byte1.
1Eh	TX_RDSD2	Transmit RDS data byte2.
1Fh	TX_RDSD3	Transmit RDS data byte3.
20h	TX_RDSD4	Transmit RDS data byte4

REGISTER	NAME	USER CONTROL FUNCTIONS
21h	TX_RDSD5	Transmit RDS data byte5
22h	TX_RDSD6	Transmit RDS data byte6
23h	TX_RDSD7	Transmit RDS data byte7
24h	PAC	PA output power target control.
25h	FDEV	Specify total TX frequency deviation.
26h	RDS	Specify transmit RDS frequency deviation.
27h	GPLT	Transmitter soft chip threshold, gain of TX pilot.
28h	REG_VGA	TX AGC gain.

Register Bit R/W Status:

RO - *R*ead *O*nly: You cannot program these bits.
WO - *W*rite *O*nly: You can write and read these bits; the value you read back will be the same as written.
R/W - *R*ead/*W*rite: You can write and read these bits; the value you read back can be different from the value written. Typically, the value is set by the chip itself. This could be a calibration result, AGC FSM result, etc.

Word: SYSTEM1 Address: 00h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
swrst	recal	stnby	rxreq	txreq	chsc	ccs_ch_dis	cca_ch_dis
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7	swrst	0	Reset all registers to default values	
			swrst	Register values
			0	Keep the current value
			1	Reset to default values
6	recal	0	Reset the state to initial states and recalibrate all blocks	
			recal	Description
			0	No action. FSM runs normally
			1	Reset the FSM. After this bit is de-asserted, FSM will go through all the power up and calibration sequence.
5	stnby	1	Request Immediately enter Standby mode whatever state chip is in. Note: "stnby" has the highest priority.	
			stnby	Modes
			0	Non standby mode.
			1	Enter standby mode
4	rxreq	0	Receiving request. In simplex mode, It overwrites TXREQ.	
			RXREQ	Modes
			0	Non RX mode.
			1	Enter Receiving mode
3	txreq	0	Transmission request	
			TXREQ	Modes

			0	Non TX mode.
			1	Enter transmit mode.
2	chsc	0	Channel Scan mode enable: Combined with RXREQ chip scans for occupied channel for receiving or empty channel for transmission. After completing channel scanning, this bit will be cleared automatically. For RX Scan, the FIRST valid channel will be selected. To start CCA/CCS, set CHSC to 1. When CCA/CCS is completed, CHSC will be cleared to 0 automatically. To use the scanned channel, set CCA_CH_DIS = 0. (CCA_CH_DIS can be set to 0 at the same time CHSC=1).	
			CHSC	Modes
			0	Normal operation
			1	Channel Scan mode operation.
1	ccs_ch_dis	1	CH (channel index selection). See description for TX_CH register for more information.	
			ccs_ch_dis	Channel Selection
			0	TX_CH is decided by internal CCS
			1	TX_CH is decided writing in TX_CH[9:0]
0	cca_ch_dis	1	CH (channel index selection). See description for RX_CH register for more information.	
			cca_ch_dis	Channel Selection
			0	RX_CH is decided by internal CCA
			1	RX_CH is decided writing in RX_CH[9:0]

Word: SYSTEM2 Address: 01h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rx_rdsen	tx_rdsen	force_mo	tx_mono	rx_mute	tx_mute	rdsrdy	tc
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7	rx_rdsen	0	Receiver RDS enable	
			rx_rdsen	Modes
			0	RDS Disable
			1	RDS Enable
6	tx_rdsen	0	Transmitter RDS enable	
			tx_rdsen	Modes
			0	RDS Disable
			1	RDS Enable
5	force_mo	0	Force receiver in MONO mode	
			force_mo	Value
			0	Not forced. ST/MONO auto selected
			1	Forced in MONO mode
4	tx_mono	0	TX stereo and mono mode selection	
			tx_mono	TX mode mono/stereo selection
			0	Stereo
			1	Mono
3	rx_mute	0	RX audio Mute enable.	
			Rx_mute	Modes
			0	Mute Disabled.
			1	Mute Enabled.

2	tx_mute	0	TX audio mute enabel Tx_mute: Modes 0: Mute Disabled. 1: Mute Enabled.
1	rdsrdy	0	RDS transmitting ready. If user want the chip transmitting all the 8 bytes in RDS0~RDS7, user should toggle this bit. Then the chip internally will fetch these bytes after completing transmitting of current group.
0	tc	1	Pre-emphasis and de-emphasis time constant TC: Time Constant (us) 0: 50 1: 75

Word: CCA **Address: 02h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
xtal_inj	imr	snr_cca_th[5]	snr_cca_th [4]	snr_cca_th [3]	snr_cca_th [2]	snr_cca_th [1]	snr_cca_th [0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7	xtal_inj	1	Select the reference clock source 0: Inject sine-wave clock 1: Inject digital clock
6	imr	0	Image Rejection. In CCA disabled mode (CCA_DIS=1), this is user set value. In CCA mode, this is CCA selection read out imr: Image rejection status 0: LO<RF, image is in lower side 1: LO>RF, image is in upper side
5:0	SNR_CCA_TH[5:0]	010000	The threshold for determination of whether current channel is valid by check its SNR. The channel could be thought of as a valid channel with SNR > SNR_CCA_TH

Word: SNR **Address: 03h**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
snrdb[7]	snrdb[6]	snrdb[5]	snrdb[4]	snrdb[3]	snrdb[2]	snrdb[1]	snrdb[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	SNRDB	rrrrrrrr	Estimated RF input CNR.

Word: RSSISIG Address: 04h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rssidb[7]	rssidb[6]	rssidb[5]	rssidb[4]	rssidb[3]	rssidb[2]	rssidb[1]	rssidb[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RSSIDB	rrrrrrr	In-band signal RSSI (Received signal strength indicator) dBuV value. dBuV=RSSI-49.

Word: CID1 Address: 05h (RO)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rsvd	rsvd	rsvd	cid1[2]	cid1[1]	cid1[0]	cid2[1]	cid2[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	value	Description	
7:5	RSVD	rrr	Reserved	
4:2	CID1[2:0]	rrr	Chip ID for product family:	
		000	000	FM
			001-111	Reserved
1:0	CID2[1:0]	rr	Chip ID for minor revision:	
		01	00	1
			01	2
			10	3
			11	4

Word: CID2 Address: 06h (RO)

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
cid3[5]	cid3[4]	cid3[3]	cid3[2]	cid3[1]	cid3[0]	cid4[1]	cid4[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Devault	Description	
7:2	CID3[5:0]	rrrrrr	Chip ID for product ID:	
		001101	001101	Transceiver – QN8066
		001111	Others	Reserved
1:0	CID4[1:0]	rr	00	1
		00	01	2
			10	3
			11	4

Word: XTAL_DIV0 Address: 07h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
xtal_div[7]	xtal_div[6]	xtal_div[5]	xtal_div[4]	xtal_div[3]	xtal_div[2]	xtal_div[1]	xtal_div[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	xtal_div[7:0]	00000001	Lower 8 bits of xtal_div[10:0]. Xtal_div[10:0] = round(freq of xtal/32.768KHz).

Word: XTAL_DIV1 Address: 08h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
pll_dlt[4]	pll_dlt[3]	pll_dlt[2]	pll_dlt[1]	pll_dlt[0]	xtal_div[10]	xtal_div[9]	xtal_div[8]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:3	pll_dlt[4:0]	00001	Lower 5 bits of pll_dlt[12:0].
2:0	xtal_div[10:8]	000	Higher 3 bits of xtal_div[10:0]. Xtal_div[10:0] = round(freq of xtal/32.768KHz)

Word: XTAL_DIV2 Address: 09h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
pll_dlt[12]	pll_dlt[11]	pll_dlt[10]	pll_dlt[9]	pll_dlt[8]	pll_dlt[7]	pll_dlt[6]	pll_dlt[5]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	pll_dlt[12:5]	01011100	higher 8 bits of pll_dlt[12:0]. Pll_dlt[12:0] = round (14.592GHz/($Freq_{xtal}$ /XTAL_DIV[10:0])) - 442368 .

Word: STATUS1 Address: 0Ah

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
fsm[3]	fsm[2]	fsm[1]	fsm[0]	rxcca_fail	rxagcset	rxstatus	st_mo_rx
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description	
7:4	FSM[3:0]	rrrr	Top FSM state code	
			FSM[3:0]	FSM status
			0000	STBY
			0001	RESET
			0010	CALI
			0011	IDLE
			0100	CALIPLL
			0101	Reserved
			0110	Reserved
			0111	TXPLLC
			1000	TX_RSTB
			1001	PACAL
			1010	TRANSMIT
			1011	TXCCA
			1100~1111	Reserved
3	rxcca_fail	r	RXCCA status flag. To indicate whether a valid channel is found during RX CCA. If a valid channel is found, channel index will stay there, and RXCCA_FAIL=0; otherwise, it will stay at the end of scan range and RXCCA_FAIL=1.	
			RXCCA_FAIL	
			0	RX CCA success to find a valid channel
			1	RX CCA fail to find a valid channel
2	RXAGCSET	r	RX AGC Settling status	
			RXAGCSET	RX AGC Status
			0	Not settled
			1	Settled
1	RXSTATUS	r	RX Status	
			RX STATUS	RX Status
			0	No receiving
			1	Receiving
0	ST_MO_RX	r	Stereo receiving status	
			STEREO	Receiving Status
			1	Mono
			0	Stereo

Word: RX_CH **Address: 0Bh**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rxch[7]	rxch[6]	rxch[5]	rxch[4]	rxch[3]	rxch[2]	rxch[1]	rxch[0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description
7:0	RXCH[7:0]	00110000	Lower 8 bits of 10-bit Channel index. Channel used for RX have two origins, one is from RXCH register (REG0EH[1:0]+REG0BH) which can be written by the user, another is from CCA. CCA selected channel is stored in an internal register, which is physically a different register with CH register, but it can be read out through register CH and be used for RX when CCA_CH_DIS(REG0[0])=0. FM channel: (60+RXCH*0.05)MHz

Word: CH_START **Address: 0Ch**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
ch_sta[7]	ch_sta[6]	ch_sta[5]	ch_sta[4]	ch_sta[3]	ch_sta[2]	ch_sta[1]	ch_sta[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	CH_STA[7:0]	00011100	Lower 8 bits of 10-bit CCA(channel scan) start channel index

Word: CH_STOP **Address: 0Dh**

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
ch_stp[7]	ch_stp[6]	ch_stp[5]	ch_stp[4]	ch_stp[3]	ch_stp[2]	ch_stp[1]	ch_stp[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	CH_STP[7:0]	11000000	Lower 8 bits of 10-bit CCA(channel scan) stop channel index

Word: CH_STEP Address: 0Eh

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
ch_fstep[1]	ch_fstep[0]	ch_stp[9]	ch_stp[8]	ch_sta[9]	ch_sta[8]	rxch[9]	rxch[8]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7:6	CH_FSTEP[1:0]	01	CCA (channel scan) frequency step	
			00	50KHz
			01	100KHz
			10	200KHz
			11	Reserved
5:4	CH_STP[9:8]	11	Highest 2 bits of 10-bit CCA(channel scan) stop channel index Stop freq is (60+RXCH_STP*0.05)MHz	
3:2	CH_STA[9:8]	10	Highest 2 bits of 10-bit CCA(channel scan) start channel index Start freq is (60+RXCH_STA*0.05)MHz	
1:0	RXCH[9:8]	10	Highest 2 bits of 10-bit channel index Channel freq is (60+RXCH*0.05)MHz	

Word: RX_RDSD0 Address: 0Fh

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rx_rdsd0[7]	rx_rdsd0[6]	rx_rdsd0[5]	rx_rdsd0[4]	rx_rdsd0[3]	rx_rdsd0[2]	rx_rdsd0[1]	rx_rdsd0[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RX_RDSD0	xxxxxxxx	RX_RDS data byte0.

Word: RX_RDSD1 Address: 10h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rx_rdsd1[7]	rx_rdsd1[6]	rx_rdsd1[5]	rx_rdsd1[4]	rx_rdsd1[3]	rx_rdsd1[2]	rx_rdsd1[1]	rx_rdsd1[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RX_RDSD1	xxxxxxxx	RX_RDS data byte1.

Word: RX_RDSD2 Address: 11h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rx_rdsd2[7]	rx_rdsd2[6]	rx_rdsd2[5]	rx_rdsd2[4]	rx_rdsd2[3]	rx_rdsd2[2]	rx_rdsd2[1]	rx_rdsd2[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RX_RDSD2	xxxxxxxx	RX_RDS data byte2.

Word: RX_RDSD3 Address: 12h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rx_rdsd3[7]	rx_rdsd3[6]	rx_rdsd3[5]	rx_rdsd3[4]	rx_rdsd3[3]	rx_rdsd3[2]	rx_rdsd3[1]	rx_rdsd3[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RX_RDSD3	xxxxxxxx	RX_RDS data byte3.

Word: RX_RDSD 4 Address: 13h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rx_rdsd4[7]	rx_rdsd4[6]	rx_rdsd4[5]	rx_rdsd4[4]	rx_rdsd4[3]	rx_rdsd4[2]	rx_rdsd4[1]	rx_rdsd4[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RX_RDSD4	xxxxxxxx	RX_RDS data byte4.

Word: RX_RDSD5 Address: 14h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rx_rdsd5[7]	rx_rdsd5[6]	rx_rdsd5[5]	rx_rdsd5[4]	rx_rdsd5[3]	rx_rdsd5[2]	rx_rdsd5[1]	rx_rdsd5[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RX_RDSD5	xxxxxxxx	RX_RDS data byte5.

Word: RX_RDSD6 Address: 15h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd5[7]	rdsd5[6]	rdsd5[5]	rdsd5[4]	rdsd5[3]	rdsd5[2]	rdsd5[1]	rdsd5[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RX_RDSD6	xxxxxxxx	RX_RDS data byte6.

Word: RX_RDSD7 Address: 16h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rdsd6[7]	rdsd6[6]	rdsd6[5]	rdsd6[4]	rdsd6[3]	rdsd6[2]	rdsd6[1]	rdsd6[0]
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7:0	RX_RDSD7	xxxxxxxx	RX_RDS data byte7.

Word: STATUS2 Address: 17h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rds_rxupd	e_det	rdsc0c1	rdssync	rdsd0err	rdsd1err	rdsd2err	rdsd3err
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description	
7	RDS_RXUPD	r	RDS RX: RDS received group updated. Each time a new group is received, this bit will be toggled. If RDS_INT_EN=1, then at the same time this bit is toggled, interrupt output will out put a 4.5 ms low pulse.	
			RDS_RXUPD	Status
			0->1 or 1->0	A new set (8 Byte) of data is received
			0->0 or 1->1	New data is in receiving
6	E_DET	r	'E' block (MMBS block) detected	
			E_DET	Status
			0	Not detected
			1	detected
5	RDSC0C1	r	Type indicator of the RDS third block in one group	
			RDSC0C1	RDS third block status
			0	C0
			1	C1
4	RDSSYNC	r	RDS block synchronous indicator	
			RDSSYNC	RDS block sync status
			0	Non-synchronous
			1	Synchronous
3	RDS0ERR	r	Received RDS block 0 status indicator	
			RDS0ERR	RDS block 0 status
			0	No error
			1	Error
2	RDS1ERR	r	Received RDS block 1 status indicator	
			RDS1ERR	RDS block 1 status
			0	No error
			1	Error
1	RDS2ERR	r	Received RDS block 2 status indicator	
			RDS2ERR	RDS block 2 status
			0	No error

			1	Error
0	RDS3ERR	r	Received RDS block 3 status indicator	
			RDS3ERR	RDS block 3 status
			0	No error
			1	Error

Word: VOL_CTL_ Address: 18h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tx_diff	dac_hold	gain_dig[2]	gain_dig[1]	gain_dig[0]	gain_ana[2]	gain_ana[1]	gain_ana[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7	TX_DIFF	0	Tx audio input mode selection TX_DIFF: Mode 0: Single ended 1: Differential
6	DAC_HOLD	0	DAC output control DAC_HOLD: DAC output 0: Normal operation 1: Hold DAC output to a fixed voltage
5:3	GAIN_DIG[2:0]	000	GAIN_DIG[2:0] set digital volume gain. 101: -5dB 100: -4dB 011: -3dB 010: -2dB 001: -1dB 000: 0dB
2:0	GAIN_ANA[2:0]	111	GAIN_ANA[2:0] set volume control gain of analog portion. 111: 0dB 110: -6dB 101: -12dB 100: -18dB 011: -24dB 010: -30dB 001: -36dB 000: -42dB

Word: INT_CTRL Address: 19h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
rds_int_en	cca_int_en	rds_only	s1k_en	rds_4k_mode	Priv_mode	txch[9]	txch[8]
wo	wo	wo	wo	wo	wo	rw	rw

Bit	Symbol	Default	Description
7	rds_int_en	0	RDS RX interrupt enable. When RDS_INT_EN=1, a 4.5ms low pulse will be output from pad din (RX mode) when a new group data is received and stored into RDS0~RDS7 (RX mode). Rds_int_en: Status 0: Disable 1: Enable
6	cca_int_en	0	RX CCA interrupt enable. When CCA_INT_EN=1, a 4.5ms low pulse will be output from pad din (RX mode) when a RXCCA (RX mode) is finished. Cca_int_en: Status 0: Disable 1: Enable
5	rds_only	1	RDS Mode rds_only: RDS Mode Selection 0: Received bit-stream have both RDS and MMBS blocks (‘E’ block) 1: Received bit-stream has RDS block only, no MMBS block (‘E’ block)
4	s1k_en	0	Internal 1K tone selection. It will be used as DAC output when RXREQ. 0: Disabled 1: Enabled
3	rds_4k_mode	0	Enable RDS RX/TX 4k Mode: with or without the privacy mode (audio scramble and RDS encryption)
2	Priv_mode	0	Private mode for RX/TX
1:0	TXCH[9:8]	10	Highest 2 bits of 10-bit channel index Channel freq is (60+TXCH*0.05)MHz

Word: STATUS3 Address: 1Ah

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
cap_sh	aud_pk[3]	aud_pk[2]	aud_pk[1]	aud_pk[0]	rds_txupd	rxagcerr	rsvd
ro	ro	ro	ro	ro	ro	ro	ro

Bit	Symbol	Default	Description
7	CAP_SH	r	Large CAP short detection flag. 1 indicates a short. This bit is the OR-ed result of Poly phase filter I path and Poly phase filter Q path.
6:3	aud_pk[3:0]	rrrr	Audio peak value at ADC input is aud_pk[3:0]*45mV
2	RDS_TXUPD	r	RDS TX: To transmit the 8 bytes in RDS0~RDS7, user should toggle the register bit RDSRDY. Then the chip internally fetches these bytes after completing transmitting of current group. Once the chip internally fetched these bytes, it will toggle this bit, and user can write in another group.
1	rxagcerr	r	RXAGC Error Flag

			rxagcerr	Status
			0	No Error
			1	Error
0	Rsvd	r	Reserved	

Word: TXCH Address: 1Bh

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
txch[7]	txch[6]	txch[5]	txch[4]	txch[3]	txch[2]	txch[1]	txch[0]
rw	rw	rw	rw	rw	rw	rw	rw

Bit	Symbol	Default	Description
7:0	TXCH[7:0]	00110000	Lower 8 bits of 10-bit Channel index. Channel used for TX have two origins, one is from TXCH register (REG19H[1:0]+REG1BH) which can be written by the user, another is from CCS. CCS selected channel is stored in an internal register, which is physically a different register with TXCH register, but it can be read out through register TXCH and be used for TX when CCS_CH_DIS(REG0[0])=0. FM channel: (60+TXCH*0.05)MHz

Word: TX_RDSD0 Address: 1Ch

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tx_rdsd0[7]	tx_rdsd0[6]	tx_rdsd0[5]	tx_rdsd0[4]	tx_rdsd0[3]	tx_rdsd0[2]	tx_rdsd0[1]	tx_rdsd0[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	TX_RDSD0	0000 0000	RDS data byte0 to be sent. Data written into RDSD0~RDSD7 cannot be sent out if user didn't toggle RDSTXRDY to allow the data loaded into internal transmitting buffer.

Word: TX_RDSD1 Address: 1Dh

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tx_rdsd1[7]	tx_rdsd1[6]	tx_rdsd1[5]	tx_rdsd1[4]	tx_rdsd1[3]	tx_rdsd1[2]	tx_rdsd1[1]	tx_rdsd1[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	TX_RDSD1	00000000	TX_RDS data byte1.

Word: TX_RDSD2 Address: 1Eh

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tx_rdsd2[7]	tx_rdsd2[6]	tx_rdsd2[5]	tx_rdsd2[4]	tx_rdsd2[3]	tx_rdsd2[2]	tx_rdsd2[1]	tx_rdsd2[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	TX_RDSD2	00000000	TX_RDS data byte2.

Word: TX_RDSD3 Address: 1Fh

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tx_rdsd3[7]	tx_rdsd3[6]	tx_rdsd3[5]	tx_rdsd3[4]	tx_rdsd3[3]	tx_rdsd3[2]	tx_rdsd3[1]	tx_rdsd3[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	00000000	TX_RDSD3	TX_RDS data byte3.

Word: TX_RDSD4 Address: 20h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tx_rdsd4[7]	tx_rdsd4[6]	tx_rdsd4[5]	tx_rdsd4[4]	tx_rdsd4[3]	tx_rdsd4[2]	tx_rdsd4[1]	tx_rdsd4[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	00000000	TX_RDSD4	TX_RDS data byte4.

Word: TX_RDSD5 Address: 21h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tx_rdsd5[7]	tx_rdsd5[6]	tx_rdsd5[5]	tx_rdsd5[4]	tx_rdsd5[3]	tx_rdsd5[2]	tx_rdsd5[1]	tx_rdsd5[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	00000000	TX_RDSD5	TX_RDS data byte5.

Word: TX_RDSD6 Address: 22h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tx_rdsd6[7]	tx_rdsd6[6]	tx_rdsd6[5]	tx_rdsd6[4]	tx_rdsd6[3]	tx_rdsd6[2]	tx_rdsd6[1]	tx_rdsd6[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	00000000	TX_RDSD6	TX_RDS data byte6.

Word: TX_RDSD7 Address: 23h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tx_rdsd7[7]	tx_rdsd7[6]	tx_rdsd7[5]	tx_rdsd7[4]	tx_rdsd7[3]	tx_rdsd7[2]	tx_rdsd7[1]	tx_rdsd7[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:0	00000000	TX_RDSD7	TX_RDS data byte7.

Word: PAC Address: 24h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
txpd_clr	pa_trgt[6]	pa_trgt[5]	pa_trgt[4]	pa_trgt[3]	pa_trgt[2]	pa_trgt[1]	pa_trgt[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7	0	TXPD_CLR	TX aud_pk clear signal. Audio peak value is max-hold and stored in aud_pk[3:0]. Once TXPD_CLR is toggled, the aud_pk value is cleared and restarted again.
6:0	1111111	PA_TRGT[6:0]	PA output power target is 0.91*PA_TRGT+70.2dBu. Valid values are 24-56.

Word: FDEV Address: 25h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
tx_fdev[7]	tx_fdev[6]	tx_fdev[5]	tx_fdev[4]	tx_fdev[3]	tx_fdev[2]	tx_fdev[1]	tx_fdev[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description	
7:0	TX_FDEV[7:0]	01101100	Specify total TX frequency deviation. TX frequency deviation = 0.69KHz*TX_FEDV.	
			TX_FDEV[7:0]	value
			00000000-11111111	0-255

Word: RDS Address: 26h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Line_in_en	rdsfdev[6]	rdsfdev[5]	rdsfdev[4]	rdsfdev[3]	rdsfdev[2]	rdsfdev[1]	rdsfdev[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7	Line_in_en	0	Audio Line-in enable control Line_in_en: Operation mode 0: Disable 1: Enable
6:0	RDSFDEV[6:0]	0000110	Specify RDS frequency deviation. RDS frequency deviation = 0.35KHz*RDSFDEV in normal mode RDS frequency deviation = 0.207KHz*RDSFDEV in 4k mode and private mode RDSFDEV[6:0]: value 0000000-1111111: 0~127

Word: GPLT Address: 27h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Tx_sftclpth[1]	Tx_sftclpth[0]	T1m_sel[1]	T1m_sel[0]	gain_txplt[3]	gain_txplt[2]	gain_txplt[1]	gain_txplt[0]
wo	wo	wo	wo	wo	wo	wo	wo

Bit	Symbol	Default	Description
7:6	Tx_sftclpth[1:0]	00	TX soft clip threshold TX_SFTCLPTH[1:0]: Value 00: 12'd2051 (3db back off from 0.5v) 01: 12'd1725 (4.5db back off from 0.5v) 10: 12'd1452 (6db back off from 0.5v) 11: 12'd1028 (9db back off from 0.5v)
5:4	t1m_sel[1:0]	10	Selection of 1 minute time for PA off when no audio. T1m_sel[1:0]: Time 00: 57s 01: 58s 10: 59s 11: Infinity (never)
3:0	GAIN_TXPLT[3:0]	1001	Gain of TX pilot to adjust pilot frequency deviation. Refer to peak frequency deviation of MPX signal when audio input is full scale. GAIN_TXPLT[3:0]: value 0111: 7% * 75KHz 1000: 8% * 75KHz 1001: 9% * 75KHz 1010: 10% * 75KHz

Word: REG_VGA Address: 28h

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)
Tx_sftclpen	Txagc_gvga[2]	Txagc_gvga[1]	Txagc_gvga[0]	Txagc_GDB[1]	Txagc_GDB[0]	rin[1]	rin[0]
wo	rw	rw	rw	rw	rw	wo	wo

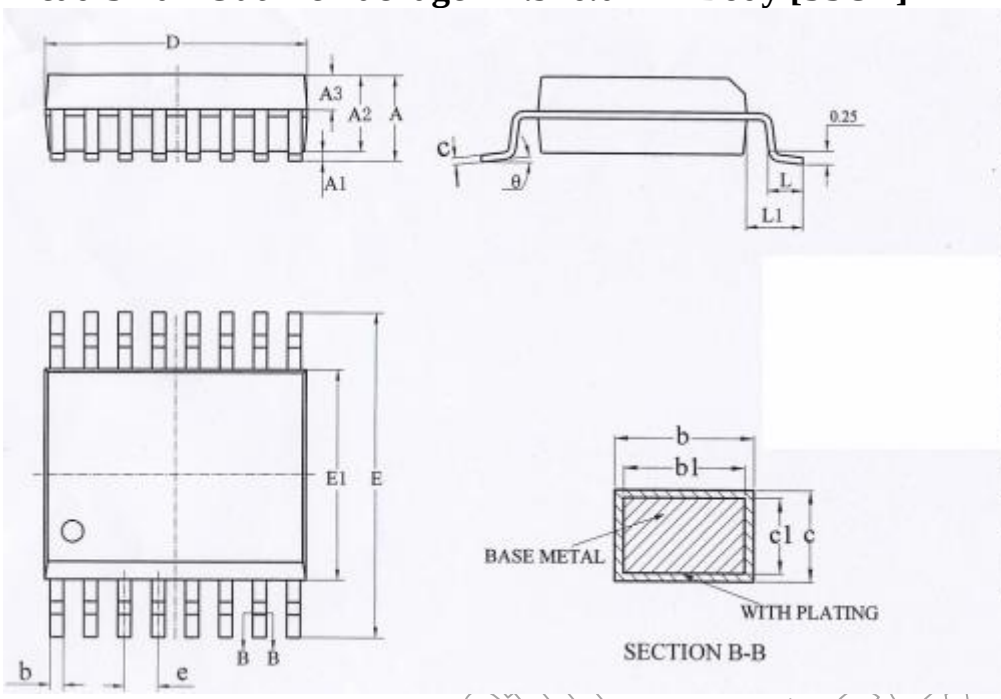
Bit	Symbol	Default	Description
7	Tx_sftclpen	0	TX soft clipping enable TX_SFTCLPEN: TX_SFTCLPEN 0: 0 1: 1
6:4	TXAGC_GVGA[2:0]	011	TX input buffer gain. TXAGC_GVGA[2:0] / RIN[1:0]: 00 / 01 / 10 / 11 000: 3 / -3 / -9 / -15 001: 6 / 0 / -6 / -12 010: 9 / 3 / -3 / -9 011: 12 / 6 / 0 / -6 100: 15 / 9 / 3 / -3 101: 18 / 12 / 6 / 0 11X: Reserved
3:2	TXAGC_GDB[1:0]	00	TX digital gain TXAGC_GDB[1:0]: Digital gain 00: 0 dB 01: 1 dB 10: 2 dB 11: Reserved
1:0	RIN[1:0]	10	TX mode input impedance for both L/R channels. RIN[1:0]: Input impedance (kΩ) 00: 10 01: 20 10: 40 11: 80

7 ORDERING INFORMATION

Part Number	Description	Package
QN8066-UCNB	The QN8066-UCNB is Single-Chip Low-Power FM transceiver.	4.9x6.0 mm Body [SSOP16]

8 PACKAGE DESCRIPTION

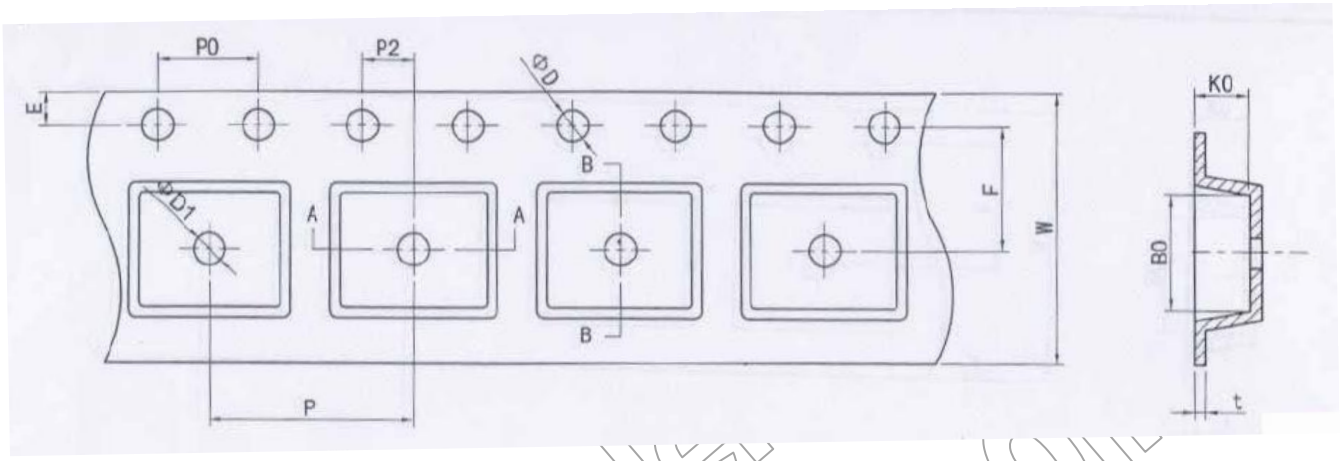
16-Lead Small Outline Package – 4.9x6.0 mm Body [SSOP]

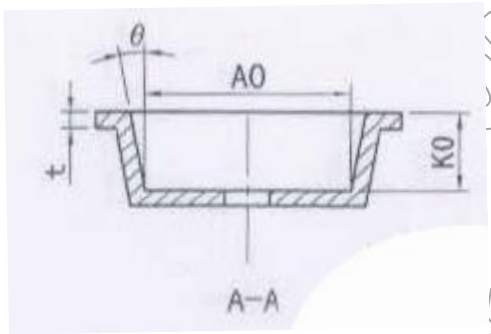


SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	0.18	0.25
A2	1.35	1.40	1.45
A3	0.50	0.60	0.70
b	0.24	—	0.30
b1	0.23	0.254	0.28
c	0.20	—	0.25
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	—	4.00
e	0.635BSC		
L	0.50	0.65	0.80
L1	1.05BSC		
θ	0	—	8°
L/F载体尺寸 (mil)	93*82 100*160		

Carrier Tape Dimensions

4.9X6.0 mm SSOP16 Carrier Tape





E	1.75±0.10
F	5.50±0.10
P2	2.00±0.05
D	1.50+0.10/−0
D1	1.50±0.10
P0	4.00±0.10
10P0	40.0±0.20

W	12.00±0.10	
P	8.00±0.10	
A0	6.60±0.10	2
B0	5.20±0.10	
K0	2.10±0.10	
t	0.30±0.05	
θ	3° TYP	3

Figure 6 SSOP16 Carrier Tape Drawing

NOTES:

1. 10 sprocket hole pitch cumulative tolerance ±0.2mm maximum.
2. Camber not to exceed 1mm in 100mm: ≤1mm/100mm.
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

9 SOLDER REFLOW PROFILE

9.1 Package Peak Reflow Temperature

QN8066 is assembled in a lead-free SSOP16 package. Since the geometrical size of QN8066 is 4.9× 6.0 × 1.75 mm, the volume and thickness is in the category of volume<350 mm^3 and 1.6 mm<thickness<2.5 mm in Table 4-, Pb-Free Process - Classification Temperatures (Tc) of IPC/JEDEC J-STD-020D. The peak reflow temperature is:

$$T_p = 260^o C$$

The temperature tolerance is +0°C and -5°C. Temperature is measured at the top of the package.

9.2 Classification Reflow Profiles

Profile Feature		Specification*
Average Ramp-Up Rate (tsmax to tP)		3°C/second max.
Pre-heat:	Temperature Min (Tsmin)	150°C
	Temperature Max (Tsmax)	200°C
	Time (ts)	60-180 seconds
Time maintained above:	Temperature (T_L)	217°C
	Time (t_L)	60-150 seconds
Peak/Classification Temperature (Tp)		260°C
Time within 5°C of Actual Peak Temperature (tp)		20-40 seconds
Ramp-Down Rate		6°C/second max.
Time 25°C to Peak Temperature		8 minutes max.

*Note: All temperatures are measured at the top of the package.

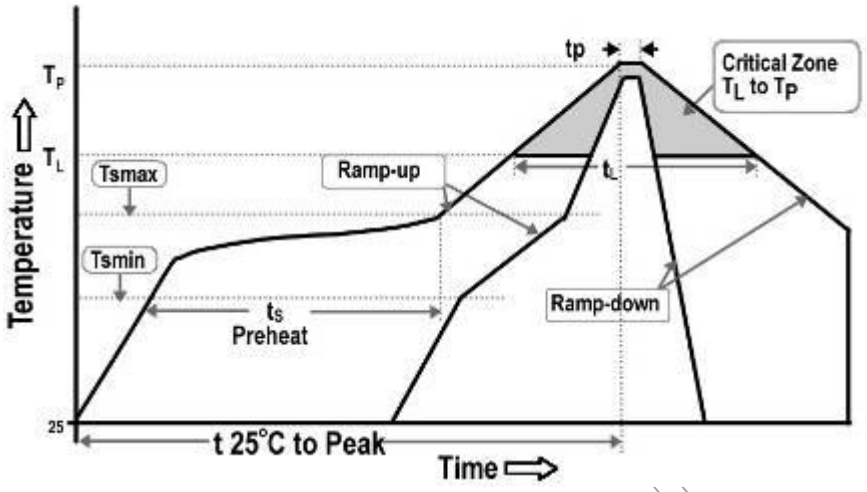


Figure 7 Reflow Temperature Profile

9.3 Maximum Reflow Times

All package reliability tests were performed and passed with a pre-condition procedure that repeats a reflow profile, which conforms to the requirements in Section 9.2, **three (3)** times.

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